10. The method as claimed in claim 7, wherein said connecting electrodes of said semiconductor chip and said wiring board by metal thin wires is performed prior to said sealing said second adhesive layer and part of said semiconductor chip with an encapsulating resin.--

REMARKS

The Examiner's Action mailed on April 24, 2002 has been received and its contents carefully considered.

In this Amendment, Applicant has editorially amended the specification, Figure 8, and claims 1-5 and 7. Further, claims 8-10 have been added to the application. Claims 1, 4, 5 and 7 are the independent claims. Claims 1-10 are pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Initially, upon review of the application, it was noted that Figure 8 was directed to a conventional arrangement. As such, submitted for the Examiner's approval are proposed drawing corrections, in which Figure 8 has been labeled as being prior art. The change is indicated in red ink. Upon approval of the drawing change and allowance of the application, revised formal drawings will be submitted in compliance with United States Patent and Trademark Office guidelines.

The Examiner has rejected claims 1 and 4 as being anticipated by *Lin* (USP 6,184,580). It is submitted that these claims are patentably distinguishable over this cited reference for at least the following reasons.

Applicant's independent claim 1 is directed to a semiconductor device which includes a semiconductor chip and metal thin wires which connect the chip to a wiring board. The chip and the wiring board are disposed on a heat spreader. The wiring board has an opening for accommodating the semiconductor chip. An adhesive layer is provided over a principle surface of a heat spreader. When the semiconductor chip is disposed in the opening of the wiring board, it is separated from edges of the wiring board that collectively define the opening by a space, so that the semiconductor chip does not completely cover the heat spreader within the opening. Further, the portion of the heat spreader within the opening which is not covered by the semiconductor chip is completely covered by the adhesive layer. Further, an encapsulating resin for sealing at least the metal thin wires is provided.

As disclosed by Applicant's specification, prior to Applicant's claimed invention and in accordance with the conventional arrangement, voids would be formed within the resin in a region of the metal thin wires 4. These voids would trap moisture, causing damage to the metal thin wires 4. Applicant's claimed invention overcomes these problems associated with the conventional arrangement by completely covering a portion of the heat spreader within the opening that is not covered by the semiconductor chip with the adhesive layer. This claimed arrangement is neither disclosed nor suggested by the cited reference.

Lin discloses a ball grid array package in which a silicone chip 20 is fixed on a surface of a heat sink 26 within a die-attach region 24. Conductive leads 36 are fixed on the surface of the heat sink using an adhesive layer 38, such as shown in Figure 2.

This reference further discloses providing a molding compound 28 to seal the bonding wires and chip.

However, and in contrast to the claimed invention, this reference does not disclose or suggest that a portion of the heat spreader within the opening that is not covered by the semiconductor chip is completely covered by an adhesive layer. As clearly shown in Figure 2, the portion of the heat sink 26 that is not covered by the chip 20 is likewise not covered by any adhesive layer. As such, this arrangement would be subjectable to voids being formed within the molding compound 28 similar to the prior art arrangement discussed in Applicant's specification. Thus, it is submitted that claim 1 has not been anticipated by or otherwise rendered obvious by this cited reference.

Applicant's independent claim 4 is submitted to be patentably distinguishable over the cited reference for similar reasons as those given above with respect to independent claim 1. In particular, this claim likewise recites that the wiring board has an opening for accommodating a semiconductor chip, with the semiconductor chip being disposed in the opening of the wiring board and being separated from edges of the wiring board, that collectively define the opening, by a space so that the chip does not completely cover the heat spreader within the opening. This claim further recites that the portion of the heat spreader within the opening that is not covered by the semiconductor chip is completely covered by the adhesive layer. As noted above, *Lin* does not disclose or otherwise suggest a portion of a heat spreader within an opening that is not covered by the semiconductor chip being completely covered by an adhesive layer, such as recited within Applicant's claim 4. As such, it is submitted that Applicant's

independent claims 1 and 4 have not been anticipated by the cited reference, and it is requested that these claims be allowed and that this rejection be withdrawn.

The Examiner has rejected claims 2 and 3 as being obvious over *Lin* and further in view of *Yamagata et al.* (USP 5,828,127). It is submitted that these claims are patentably distinguishable over the cited references for at least the following reasons.

Dependent claims 2 and 3 depend from independent claim 1. As noted above, *Lin* does not disclose or otherwise suggest the features recited within independent claim 1. Similarly, *Yamagata et al.* do not disclose or otherwise suggest these features. *Yamagata et al.* is simply directed to a semiconductor substrate in which a chip 4 is fixed on a surface of the substrate 1 by a bonding material 5, and a main package body 2 is fixed on a surface of the bonding material 5 as shown in Figure 8. However, this reference does not overcome the above-noted deficiencies of *Lin*, since this reference likewise does not disclose or suggest a portion of a heat spreader within an opening that is not covered by the semiconductor chip being completely covered by an adhesive layer, as recited by claim 1. As such, dependent claims 2 and 3 are submitted to be patentably distinguishable over the cited combination of references for at least the same reasons as independent claim 1, from which these claims depend, as well as for the additional features recited therein. It is requested that these claims be allowed and that this rejection be withdrawn.

The Examiner has further rejected claims 5-7 as being obvious over *Lin* in view of *Yamagata et al.*, and further in view of *Moscicki* (USP 6,064,115). It is submitted that these claims are patentably distinguishable over the cited references for at least the following reasons.

Applicant's independent claim 5 is directed to a method of making a semiconductor device which includes, *inter alia*, sealing a second adhesive layer and part of a semiconductor chip with a first encapsulating layer and, after the first encapsulating resin has been cured, sealing metal thin wires and the semiconductor chip with a second encapsulating resin. This claimed method corresponds to the fourth embodiment, and ensures that no voids occur while reducing the cost of manufacture (see page 17, first two paragraphs).

In contrast, none of the cited references disclose performing first and second sealing operations, much less performing a second sealing operation after a first encapsulating resin has been cured, as recited by Applicant's independent claim 5. In fact, the Examiner's Action has not even addressed this claimed feature. As such, it is submitted that independent claim 5 and dependent claim 6 are *prima facie* patentably distinguishable over the cited references.

Further, independent claim 7 is submitted to be patentably distinguishable over the cited references in that this claim recites sealing a second adhesive layer and part of a semiconductor chip with an encapsulating resin, and after the encapsulating resin has at least partially cured, sealing metal thin wires and a semiconductor chip with more of the encapsulating resin. As noted above, the cited references do not disclose or suggest performing two (2) sealing operations, and therefore, the Examiner's Action has not established a *prima facie* case of obviousness against independent claim 7. Thus, it is requested that these claims be allowed and that these rejections be withdrawn.

Applicant has further added claims 8-10, which are submitted to be patentably distinguishable over the cited references for at least the same reasons as the

independent claims from which these dependent claims respectively depend, as well as for the additional features recited therein. It is requested that these claims additionally be allowed.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

July 19, 2002
Date

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please amend the specification as follows:

Page 2, please replace the second paragraph bridging lines 7-18 with the following replacement paragraph:

--This type of semiconductor device includes a semiconductor chip 1 on which, although not illustrated in the drawing, circuits and bonding pads are formed, a multi-layer wiring substrate or board 2 on which, although not shown in the drawing, bonding posts, circuits and through holes are formed in positions corresponding to the respective pads, a heat spreader 3 to which the semiconductor chip 1 and the wiring board 2 are fixed, metal thin wires 4 for connecting the pads and the posts respectively, and an encapsulating resin 5 for sealing the parts inclusive of the semiconductor chip 1 and the metal thin wires 4.--

Page 3, please replace the second paragraph bridging lines 10-15 with the following replacement paragraph:

--Defoaming is performed as needed upon charging of the encapsulating resin 5 to break or vanish foam which remain in the encapsulating resin 5, and a uniform sealed portion is formed after its curing, whereby a semiconductor device free of a reduction in reliability due to [a moisture's trap] trapped moisture or the like is completed.--

Page 8, line 10, through Page 9, line 6, please replace the paragraphs with the following replacement paragraphs:

--For example, a B-staged epoxy resin used as the B-staged thermosetting resin needs care such as the need for cold storing processing to manage its reaction probability. However, the B-staged epoxy resin can be expected to have high adhesion. Further, the thermoplastic resin is easy to [perform handling] handle, and the mixed material has characteristics of the two referred to above.

While the semiconductor chip 1 is fixedly secured to the heat spreader 3 by the adhesive layer 12 [other] rather than with the conventional die attach material, a high thermal-conductive adhesive is also known and can be also set to the same thermal conductivity as the die attach material. Even in the case of the die attach material and the adhesive, no serious influence occurs in terms of a heat dissipation property of a package.

According to the first embodiment as described above, since the semiconductor chip 1 and the wiring board 2 are fixed to the heat spreader 3 by the adhesive layer 12 provided over the entire principal surface of the heat spreader 3, the conventional recessed portion of adhesive [no occurs] does not occur between the wiring board 2 and the heat spreader 3, so that voids can be prevented from occurring in an encapsulating process step.--

Page 11, line 27, through Page 12, line 10, please replace the paragraphs with the following replacement paragraphs:

--According to the second embodiment as described above, since the adhesive layers 12 and 14 are identical in thermal characteristic and are formed over the principal surface and reverse side of the heat spreader 3, in addition to the effect obtained in the first embodiment, warpage can be reduced even if the heat spreader 3 and the adhesive layers 12 and 14 are different in thermal expansion characteristic from one another[, thus making it] . It is thus possible to realize a semiconductor device wherein a wiring board 2 and the heat spreader 3 [are] have good [in] adhesive [property] properties and a reduction in warpage is reached.--

Page 14, line 23, through Page 15, line 5, please replace the paragraphs with the following replacement paragraphs:

--In a process step (a), a frame-shaped first adhesive layer 16 is formed over the principal surface of the heat spreader 3. The wiring board 2 is fixed to the heat spreader 3 with [a] the first adhesive layer 16 interposed therebetween.

At this time, the first adhesive layer 16 is formed so as to be [become] narrower than the wiring board 2 in width to avoid an extended-out portion thereof. However, a recessed portion 17 of an adhesive occurs due to such formation.--

Page 19, please replace the second paragraph bridging lines 18-22 with the following replacement paragraph:

--Since the encapsulation is done after the bonding using the metal thin wires 4 in the fifth embodiment, the pads won't become [no] dirty and a bad influence on wire

bonding can be avoided, thus making it possible to improve the reliability of connections of the wiring portions.--

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A semiconductor device, comprising:

a semiconductor chip;

metal thin wires respectively connected to electrodes on said semiconductor chip;

a wiring board having an opening for accommodating said semiconductor chip and being electrically connected to said semiconductor chip by said metal thin wires;

a heat spreader [equipped with] having said semiconductor chip and said wiring board provided thereon;

an adhesive layer which is provided over a principle surface of said heat spreader and bonds said semiconductor chip and said wiring board to each other; and

an encapsulating resin for sealing at least said metal thin wires,

wherein said semiconductor chip is disposed in the opening of said wiring board, and is separated from edges of said wiring board that collectively define the opening by a space so that said semiconductor chip does not completely cover said heat spreader within the opening, and

wherein a portion of said heat spreader within the opening that is not covered by said semiconductor chip being completely covered by said adhesive layer.

2. (Amended) The semiconductor device as claimed in claim 1, [wherein] further comprising a second adhesive layer having the same thermal characteristic as said adhesive layer [is] provided over the reverse surface of said heat spreader.

3. (Amended) The semiconductor device as claimed in claim 2, [wherein] further comprising a radiating fin [is] provided over said second adhesive layer.

4. (Amended) A method of manufacturing a semiconductor device, comprising the following steps:

[a step for] preparing a heat spreader;

[a step for] forming an adhesive layer over a principal surface of said heat spreader;

[a step for forming] disposing a semiconductor chip and a wiring board over said adhesive layer, the wiring board having an opening for accommodating said semiconductor chip, said semiconductor chip being disposed in the opening of said wiring board, and being separated from edges of said wiring board that collectively define the opening by a space so that said semiconductor chip does not completely cover said heat spreader within the opening, a portion of said heat spreader within the opening that is not covered by said semiconductor chip being completely covered by said adhesive layer;

[a step for] connecting electrodes of said semiconductor chip and said wiring board by metal thin wires; and

[a step for] sealing at least said metal thin wires with an encapsulating resin.

5. (Amended) A method of manufacturing a semiconductor device, comprising the following steps:

[a step for] preparing a heat spreader;

[a step for] forming a first adhesive layer and a second adhesive layer over a principal surface of said heat spreader;

[a step for] forming a wiring board over said first adhesive layer;

[a step for] forming a semiconductor chip over said second adhesive layer;

[a step for] connecting electrodes of said semiconductor chip and said wiring board by metal thin wires; [and]

[a step for] sealing said second adhesive layer and part of said semiconductor chip with a first encapsulating resin; and

sealing said metal thin wires and said semiconductor chip with a second encapsulating resin after said first encapsulating resin has been cured.

7. (Amended) A method a manufacturing a semiconductor device, comprising the following steps:

[a step for] preparing a heat spreader;

[a step for] forming a first adhesive layer and a second adhesive layer over a principal surface of said heat spreader;

[a step for] forming a wiring board over said first adhesive layer;

[a step for] forming a semiconductor chip over said second adhesive layer;

[a step for] connecting electrodes of said semiconductor chip and said wiring board by metal thin wires;

[a step for] sealing said second adhesive layer and part of said semiconductor chip with an encapsulating resin; and

[a step for] after said encapsulating resin has at least partially cured, sealing said metal thin wires and said semiconductor chip with more of said encapsulating resin [after said encapsulating resin has been cured].